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**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
LP	6,399,441	6/4/2002	Ogura			
	6,388,293	5/14/02	Ogura, et al.			
	6,011,725	1/4/00	Eitan			
	6,256,231	7/3/01	Lavi, et al.			

**FOREIGN PATENT DOCUMENTS**

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
LP	2001-230332	8/24/01	Japan				
	2002-26149	1/25/02	Japan				
	2001-357681	12/26/01	Japan				
	2001-512290	8/21/01	Japan				
	2001-156189	6/8/01	Japan				

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)

LP		A Novel 2-bit/cell MONOS Memory Device with a Wrapped-Control-Gate Structure that Applies Source-Side Hot Electron Injection by Hideto Tomiye et al., 2002 Symposium on VLSI Technology Digest of a Technical papers, pp 206-207.

EXAMINER

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5/27/04

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.